Maharashtra State Board of Technical Education, Mumbai
Laboratory Plan (LP-PR)/ Course Information Sheet (CIS)

K-2

Academic Year: 2026-27 **Date:** 30/06/2026
Institute Name: K. K. Wagh Polytechnic, Nashik **MSBTE Code:** 0078
Program and Code: Computer Technology (CM) **Course Code &. Abbr.:** 313303 (DTE)
Course Name: Digital Techniques (DTE-313303) **Name of Faculty:** Mr. M.N.Jadhav
Class: SYCM-Lin **Semester:** 3rd **Scheme:** K **Course Index:** CI 303 **Learning Hrs: 15**

• Teaching-Learning & Assessment Scheme:

Title	Course Code / Abbr	Course Category	Learning Scheme					Credits	TH Paper Duration (Hrs.)	Assessment Scheme										
			Actual Contact Hrs/Week			SLH	NLH			Theory				Based on LL & TSL Practical				Based on SL		Total Marks
			CL	TL	LL					FA TH	SA TH	Total		FA-PR		SA-PR		SLA		
										Max	Max	Max	Min	Max	Min	Max	Min	Max	Min	
Digital Techniques	313303/ DTE	DSC	3	--	2	1	6	3	3	30	70	100	40	25	10	25#	10	25	10	175

Abbreviations: CL- Class Room Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS – Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination, @$ Internal Online Examination

• Course Outcomes (COs): Theory & Practical

By learning course Database Management System (DMS-313315) Second Year students will be able to:

CO No.	Course Outcomes (COs) / Unit Outcomes (UOs)
CO303.1(CO1)	Apply number system and codes concept to interprete working of digital systems.
CO303.2(CO2)	Apply Boolean laws to minimize complex Boolean function.
CO303.3(CO3)	Develop combinational logic circuits for given applications.
CO303.4(CO4)	Develop sequential logic circuits using Flip-flops.
CO303.5(CO5)	Interpret the functions of data converters and memories in digital electronic systems.

• COs, Practical Laboratory Learning Outcome (LLOs) and Mapping:

Pr. No	COs	LLO	Practical -Laboratory Learning Outcome (LLO)
PR 1	CO303.2 (CO2)	LLO 1.1	Test the functionality of basic gates & special gates
PR 2	CO303.2 (CO2)	LLO 2.1	Test the functionality ofNAND and NOR gate using bread board.
PR 3	CO303.2 (CO2)	LLO 3.1	Test the functionality of theconstruct Basic gates using universal gates.
PR 4	CO303.2 (CO2)	LLO 4.1	Construct Ex-OR, EX- NOR gates using universal gates.
PR 5	CO303.2 (CO2)	LLO 5.1	Build the logic circuit onbreadboard to verify the De -Morgan's theorems.
PR 6	CO303.3 (CO3)	LLO 6.1	Verify the truth table of Half and Full adder circuits for thegiven input.
PR 7	CO303.3 (CO3)	LLO 7.1	Verify the truth table ofHalf and Full subtractor using Boolean Expressions.
PR 8	CO303.3 (CO3)	LLO 8.1	Construct and test BCD to7 segment decoder using Digital IC
PR 9	CO303.3 (CO3)	LLO 9.1	Build/Test 2 or 4 bit Magnitude comparator using Digital IC
PR 10	CO303.3 (CO3)	LLO 10.1	Build / test function of MUX Digital IC.
PR 11	CO303.3 (CO3)	LLO 11.1	Build / test function of DEMUX Digital IC.
PR 12	CO30.3 (CO4)	LLO 12.1	Test functionality of RSflip flop using NAND Gate .
PR 13	CO303.3 (CO4)	LLO 13.1	Test functionality of Master Slave (MS) JK flip-flop using Digital IC.
PR 14	CO303.3 (CO4)	LLO 14.1	Test functionality andtruth table for D and T Flip flop.
PR 15	CO303.3 (CO4)	LLO 15.1	Interpret timing diagramof 4 bit Universal Shift Register.
PR 16	CO303.3 (CO4)	LLO 16.1	Interpret timing diagram of 4-bit ripple counter using Digital IC.
PR 17	CO303.3 (CO4)	LLO 17.1	Interpret timing diagramof Decade counter (Mod-10).
PR 18	CO303.4 (CO5)	LLO 18.1	Build R-2R resistive network on breadboard to convertgiven digital data into analog.

- **LLO-CO Mapping with PO, PSO**

LLOs		COs	POs							PSOs	
			PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PSO1	PSO2
Test the functionality of basic gates & special gates	LLO 1.1	CO303.2 (CO1)	2	–	2	–	–	–	2	2	3
Test the functionality of NAND and NOR gate using bread board.	LLO 2.1	CO303.2 (CO2)	2	–	2	–	–	–	2	2	3
Test the functionality of theconstruct Basic gates using universal gates.	LLO 3.1	CO303.2 (CO3)	2	–	2	–	–	–	2	2	3
Construct Ex-OR, EX-NOR gates using universal gates.	LLO 4.1	CO303.2 (CO3)	2	–	2	–	–	–	2	2	3
Build the logic circuit on breadboard to verify the De -Morgan's theorems.	LLO 5.1	CO303.2 (CO3)	2	–	2	–	–	–	2	2	3
Verify the truth table of Half and Full adder circuits for thegiven input.	LLO 6.1	CO303.3 (CO3)	3	2	3	2	–	1	2	2	3
Verify the truth table of Half and Full subtractor using Boolean Expressions. Boolean expressions.	LLO 7.1	CO303.3 (CO3)	3	2	3	2	–	1	2	2	3
Construct and test BCD to7 segment decoder using Digital IC	LLO 8.1	CO303.3 (CO3)	3	2	3	2	–	1	2	2	3
Build/Test 2 or 4 bit Magnitude comparator using Digital IC Magnitude comparator using DigitalIC.	LLO 9.1	CO303.3 (CO3)	3	2	3	2	–	1	2	2	3
Build / test function of MUX Digital IC.	LLO 10.1	CO303.3 (CO3)	3	2	3	2	–	1	2	2	3
Build / test function of DEMUX Digital IC.	LLO 11.1	CO303.3 (CO3)	3	2	3	2	–	1	2	2	3
Test functionality of RS flip flop using NAND Gate .	LLO 12.1	CO303.4 (CO3)	3	2	3	2	–	1	2	2	3
Test functionality of Master Slave (MS) JK flip-flop using Digital IC.	LLO 13.1	CO303.4 (CO3)	3	2	3	2	–	1	2	2	3
Test functionality and truth table for D and T Flip flop.	LLO 14.1	CO303.4 (CO3)	3	2	3	2	–	1	2	2	3
Interpret timing diagram of 4 bit Universal Shift Register.	LLO 15.1	CO303.4 (CO3)	3	2	3	2	–	1	2	2	3
Interpret timing diagram of 4-bit ripple counter using Digital IC.	LLO 16.1	CO303.4 (CO3)	3	2	3	2	–	1	2	2	3
Interpret timing diagram Decade counter (Mod-10.	LLO 17.1	CO303.4 (CO3)	3	2	3	2	–	1	2	2	3
Build R-2R resistive network on breadboard to convertgiven digital data into analog.	LLO 18.1	CO303.5 (CO4)	2	–	2	2	1	1	2	2	3

- **Practical Plan**:

Sr No	COs and LLOs	Practical Titles	Planned Dates		Remark & Faculty Sign with Assessment Date
			From	To	
1	CO1,CO2 LLO 1.1	* Test the functionality of AND, OR, NOT, Ex-OR and EX-NOR logic Gates using equivalent 74 series or CMOS Devices series.	A-04/07/2026 B-02/07/2026 C-03/07/2026	A-09/07/2026 B-10/07/2026 C-11/07/2026	
2	CO2 LLO 2.1	* Test the functionality of the given Universal Gates using equivalent 74 series /CD series.	A-09/07/2026 B-10/07/2026 C-11/07/2026	A-16/07/2026 B-17/07/2026 C-18/07/2026	
3	CO2 LLO 3.1	* Construct Basic Gates using Universal Gates.	A-16/07/2026 B-17/07/2026 C-18/07/2026	A-23/07/2026 B-24/07/2026 C-25/07/2026	
4	CO2 LLO 4.1	Construct Exclusive Gates using Universal Gates.	A-16/07/2026 B-17/07/2026 C-18/07/2026	A-23/07/2026 B-24/07/2026 C-25/07/2026	
5	CO2 LLO 5.1	* Verify De-Morgan's Theorem (1 and 2).	A-23/07/2026 B-24/07/2026 C-25/07/2026	A-01/09/2026 B-30/08/2026 C-31/08/2026	
6	CO3 LLO 6.1	* Implement 2 inputs, 3 input Adder Circuit.	A-01/09/2026 B-30/08/2026 C-31/08/2026	A-08/08/2026 B-06/08/2026 C-07/08/2026	
7	CO3 LLO 7.1	Implement 2 inputs, 3 input Subtractor Circuit.	A-08/08/2026 B-06/08/2026 C-07/08/2026	A-22/08/2024 B-13/08/2024 C-14/08/2024	
8	CO3 LLO 8.1	Test the output of BCD to 7 Segment Decoderusing Digital IC for the given inputs.	A-22/08/2024 B-13/08/2024 C-14/08/2024	A-22/09/2026 B-20/08/2026 C-21/08/2026	
9	CO3 LLO 9.1	Check the output of comparator circuit consisting of Digital IC.	A-22/08/2026 B-20/08/2026 C-21/08/2026	A-27/08/2026 B-28/08/2026 C-29/08/2026	
10	CO3 LLO 10.1	* Build and test the functionality of 4:1/8:1 Multiplexer.	A-27/08/2026 B-28/08/2026 C-29/08/2026	A-05/09/2026 B-03/09/2026 C-04/09/2026	
11	CO3 LLO 11.1	Build and test the functionality of 1:4/1:8 De-Multiplexer.	A-05/09/2026 B-03/09/2026 C-04/09/2026	A-10/09/2026 B-11/09/2026 C-12/09/2026	
12	CO4 LLO 12.1	Implement and verify the truth table of RS Flipflop.	A-10/09/2026 B-11/09/2026 C-12/09/2026	A-19/09/2026 B-17/09/2026 C-18/09/2026	
13	CO4 LLO 13.1	Implement and test the functionality of master slave- JK Flip Flop using Digital IC.	A-19/09/2026 B-17/09/2026 C-18/09/2026	A-19/09/2026 B-17/09/2026 C-18/09/2026	
14	CO4 LLO 14.1	Use Digital IC to construct and test thefunctionality of D and T flip flop.	A-19/09/2026 B-17/09/2026 C-18/09/2026	A-26/09/2026 B-24/09/2026 C-25/09/2026	
15	CO4 LLO 15.1	Build 4- bit Universal Shift register and observethe timing diagram.	A-26/09/2026 B-24/09/2026 C-25/09/2026	A-03/09/2026 B-01/09/2026 C-03/09/2026	
16	CO4 LLO 16.1	Implement Ripple Counter using Digital IC.	A-03/09/2026 B-01/09/2026 C-03/09/2026	A-03/10/2026 B-01/10/2026 C-03/10/2026	
17	CO4 LLO 17.1	* Implement Decade Counter Using Digital IC.	A-03/10/2026 B-01/10/2026 C-03/10/2026	A-08/10/2026 B-09/10/2026 C-10/10/2026	
18	CO5 LLO 18.1	* Test the output of given R-2R type Digital to Analog Converter for the given input.	A-08/10/2026 B-09/10/2026 C-10/10/2026	A-15/10/2026 B-16/10/2026 C-17/10/2026	

- **Formative & Summative Assessment Criteria:**

- **Theory Assessment:**

a) Formative assessment (TH-FA) :

- Two offline class tests each of 30 marks will be conducted as per MSBTE guidelines. The average of two class test marks will be consider for final TH-FA(Average) out of 30 marks.

b) Summative Assessment (TH- SA) :

- The comprehensive End semester assessment will be done by MSBTE by a Theory written Examination for 70 marks. Question Paper and Assessment is performed by MSBTE.
- Final Theory Score out of 100 Marks will be derived as the total score as below:
  TH-SA [out of 70] + TH- FA [Average out of 30] = 100 Marks

- **Practical Assessment:**

1. Formative Assessment (FA) of each practical/experiment will be performed progressively for 50 marks. The assessment will be performed based on the Regularity in Practical Performance, Tool Selection Ability, Use of Appropriate tool to perform the Identified tasks, Algorithm/Solution developed, Quality of output achieved, Answer to sample questions and Submit report in total time.
2. Final Term Work (FA-PR) of 25 marks is calculated based on scores in Formative Assessment for all practical's/experiments as:
   Term Work Marks = (Sum of Total Marks Scored in FA / Total Number of Experiments)*25
3. Self-learning Activities (SLA) includes Micro project / Assignment / other activities related to subject/course and it will be evaluated out of 25 Marks.
4. A Summative (comprehensive) Assessment (SA-PR) of Practical will be performed as End Semester Examination (ESE). The SA-PR will be for 25 Marks with MSBTE guidelines at the end of semester. The schedule of MSBTE Practical ESE will be display on Notice board prior to examination.

- **References :**

1. **Suggested Books for Reference:**

Sr. No.	Title of Book	Author	Publication
1	Jain R.P	Modern Digital Electronics	McGraw-Hill Publishing, New Delhi,2009 ISBN:9780070669116
2	Anand Kumar	Fundamentals of Digital Circuits	PHI learning Private limited, ISBN:978-81-203-5268-1
3	Salivahanan S, Arivazhagan S.	Digital Circuits and Design	Vikas Publishing House, New Delhi,2013ISBN: 9789325960411
4	Puri.V.K	Digital Electronics	McGraw-Hill Publishing, New Delhi,2016 ISBN:97800746331751
5	Malvino A.P Donald .P. Leach	Digital Principles	McGraw-Hill Education, New DelhiISBN:9789339203405
6	Anil.K.Maini	Digital Electronics: Principles, Devices and Applications	Wiley India, Delhi, 2007, ISBN:9780470032145
7	Floyd, Thomas	Digital Fundamentals	Pearson Education India, Delhi 2014,ISBN:9780132737968
8	G.K.Kharate	Digital Electronics	Publisher: Oxford University Press, ISBN:9780198061830

2. Software Learning Websites:

Sr. No.	Link / Portal	Description
1	https://studytronics.weebly.com/digital-electronics.html	Basics of Digital Electronics
2	https://www.udemy.com/course/basics-of-digital-techniques/	Introduction To Digital Number System & Logic Gates
3	https://www.geeksforgeeks.org/synchronous-sequential-circuits-in-digital-logic/	Boolean Algebra and Logic Gates, Combinational and Sequential Logic Circuits
4	https://onlinecourses.nptel.ac.in/noc19_ee51/preview	Digital Circuits
5	https://de-iitr.vlabs.ac.in/	Virtual Labs for Digital Systems
6	https://www.tutorialspoint.com/digital_circuits/digital_circuits_sequential_circuits.htm	Sequential Circuits

3. URLs of Referred Videos:

Sr. No.	Link / Portal	Description
1	https://youtu.be/0lwhoQ5aQe8?si=bY2vqIHmhr4R2_jp	Logic Gates Introduction
2	https://youtu.be/QIyugGzih4k?si=dcauWHRmoN7x_ImN	Binary Code Conversion System
3	https://youtu.be/LTtuYeSmJ2g?si=pF81TD8G7QuCTmHf	Latch & Flip Flop
4	https://youtu.be/fLN1YOmuAr8?si=t_Iu8fr0EvFtnhdf	Sequential Circuits
5	https://youtu.be/NjMX4hohyRI?si=DTAAtybNP2LCCnff	Shift Register

Mr. M.N.Jadhav
(Name & signature of staff)

Mr. A.D.Talole
CIAAN Co-ordinator

Prof. M.P.Bhosale
(Name & signature of HOD)

CC-

1. Lab File
2. DTE – 313303 Course File
3. Notice Board / ERP
4. Institute Website / CIAAN Coordinator
5. Progressive Assessment